REMARKS

Claims 1, 3, 5, 7, 9, 11, 17 and 19 are pending in the present application.

REQUEST FOR WITHDRAWAL OF FINALITY OF THE OFFICE ACTION

Applicant respectfully requests the withdrawal of the finality of the rejection raised in the present Office Action following the Request for Continued Examination.

The Examiner asserts that all present claims of the application are drawn to the same invention as the invention claimed before the previous amendment.

However, claim 1 was amended to incorporate additional subject matter. Therefore, claims 3, 5, 7, 9, 11, 17 and 19 dependent from claim 1 (and incorporating the subject matter of claim 1) claim different inventions that the respective claims before the previous amendment.

Therefore, the dependent claims 3, 5, 7, 9, 11, 17 and 19 are not drawn to the same invention as the invention claimed before the previous amendment. It is noted that the Examiner has changed the grounds for rejection of these claims.

Accordingly, the finality of the Office Action is improper.

REJECTION OF CLAIMS

Claims 1, 3, 5, 9, 17 and 19 have been rejected under 35 U.S.C. 103 as being unpatentable over the Fujiwara publication in view of the Hallnor publication. Claims 7 and 11 have been rejected under 35 U.S.C. 103 as being unpatentable over the Fujiwara publication in view of the Hallnor publication, and further in view of Handy.

Independent claim 1 recites a cache memory system including a small-capacity cache memory which enables high-speed access and is provided between a processor and a main memory. The system comprises:

-a software cache controller which performs software control for controlling data transfer to the cache memory in accordance with a preliminarily programmed software; and

-a hardware cache controller which performs hardware control for controlling data transfer to the cache memory by using a predetermined hardware.

The processor causes the software cache controller to perform the software control but causes the hardware cache controller to perform the hardware control when it becomes impossible to perform the software control. When a cache miss happens at the time of the software control, the processor automatically causes the hardware cache controller to perform the hardware control.

The claim specifies that the hardware cache controller performs line management of the cache memory by using a set-associative method for multiple ways and the software cache controller performs line management of the cache memory by using a fully associative method for at least one way in the multiple ways.

The Examiner admits that the Fujiwara publication does not disclose the claimed line management performed by the hardware and software cache controllers. However, he relies upon the Hallnor publication (Section 2, paragraphs 1, 3 and 4) for disclosing that "hardware controlled management is better suited for a low-associativity cache (i.e. multi-way set-associative)...., and software controlled management is better for fully-associative cache."

Considering Hallnor, the reference discloses that in some areas, a fully-associative software managed secondary cache offers an advantage over low-associativity, hardware-managed organizations.

However, the reference does not suggest hardware management by using a set-associative method for multiple ways and the software management by using a fully associative method for at least one way in the multiple ways.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As discussed above, the reference combination proposed by the Examiner suggests that in some areas, a fully-associative software managed secondary cache offers an advantage over low-associativity, hardware-managed organizations.

However, the combination of references would not suggest the claimed combination of the hardware cache controller that performs line management of the cache memory by using a set-associative method for multiple ways, and the software cache controller that performs line management of the cache memory by using a fully associative method for at least one way in the multiple ways.

Accordingly, the reference combination is not sufficient to suggest the claimed subject matter.

Moreover, it is respectfully submitted that Hallnor expressly **teach away** from the claimed invention, thereby constituting further **evidence of nonobviousness**. ***In re Bell***, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); ***In re Hedges***, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); ***In re Marshall***, 578 F.2d 301, 198 USPQ 344 (CCPA 1978).

Hallnor teaches that a fully-associative software managed secondary cache offers an advantage over low-associativity, hardware-managed organizations. Therefore, Halnor suggests using the software management instead of the software management, rather than utilizing a combination of the hardware and software cache controllers in the manner recited in claim 1.

Hence, Hallnor teaches away from the claimed combination.

The Examiner has apparently failed to give adequate consideration to the particular problems and solution addressed by the claimed invention. ***Northern Telecom, Inc. v. Datapoint Corp.***, 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); ***In re Rothermel***, 276 F.2d 393, 125 USPQ 328 (CCPA 1960). Specifically, for software control, locations for storing cache lines in a cache memory and management of the cache lines are different than for hardware control. Usually, when the software control is automatically switched to the hardware control, some of the cache lines in the cache memory, that have content different from the content of the main memory, are completely written back into the main memory and then, all the cache lines are invalidated. This causes an extremely large overhead for the processing, resulting in deterioration of efficiency.

By contrast, claim 1 recites that the management of the cache lines by the software control is performed by a set-associated method for multiple ways, the cache lines management by the hardware control is performed by using a fully associative method for at least one way in the multiple ways.

For example, the software control may perform management of the cache lines by the set-associated method for the first to third ways of the four ways in the same manner as the hardware control, which may perform the cache lines management by the fully associated method only for the fourth way of the four ways. Therefore, when the software control is automatically switched to the hardware control, the write back and invalidation may be performed only for the fourth way. As a result, the overhead in this example is reduced to one fourth of the conventional method described above.

Hence, the present invention makes it possible to reduce deterioration of efficiency caused by automatic switching from the software control to the hardware control.

The applied references do not address the problem and solution addressed by the claimed invention.

Accordingly, Applicant submits that the lack of a teaching of the claimed subject matter and the lack of any motivation for the proposed combination of references to arrive at the claimed invention, coupled with the particular problems addressed and solved by the claimed invention, undermine the basis for the Examiner's rejection of claims 1, 3, 5, 7, 9, 11, 17 and 19 under 35 U.S.C. § 103. Applicant, therefore, respectfully submits that the rejection under 35 U.S.C. § 103 is improper and should be withdrawn.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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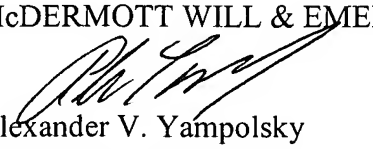

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